| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Changes in accordance with NOR 5962-R218-92 | 92-06-09 | William J. Johnson |
| B | Updated boilerplate for 5 year review. - lhl | 11-10-31 | Charles F. Saffle |

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | B | B | B | B | B | B | B | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | | | | | | | | | | | | | |

| REV STATUS | REV | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Kenneth Rice, Jr.

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.landandmaritime.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
90-05-09

REVISION LEVEL
B

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ONE TIME PROGRAMMABLE, ASYNCHRONOUS REGISTERED PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

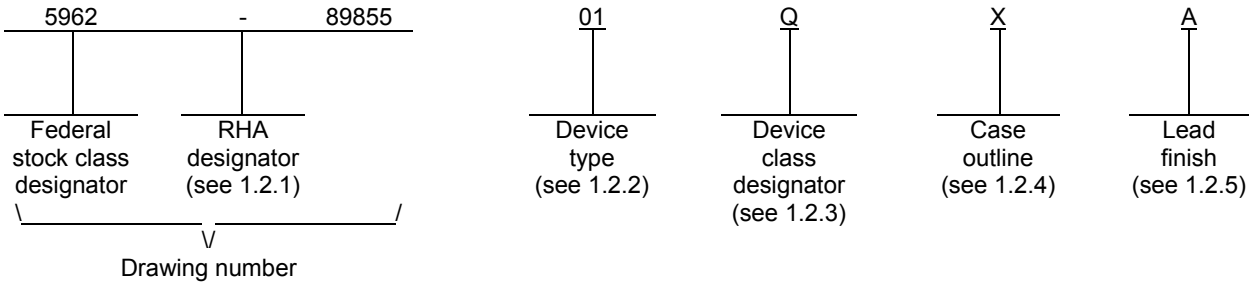
| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-89855** |

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function | Access time |
|---|---|---|---|
| 01 | CY7C331-40 | Asynchronous Registered PLD | 40 ns |
| 02 | CY7C331-30 | Asynchronous Registered PLD | 30 ns |
| 03 | CY7C331-25 | Asynchronous Registered PLD | 25 ns |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | See Figure 1 | 28 | dual-in-line package |
| Y | GDFP2-F28 | 28 | flat package |
| Z | See Figure 1 | 28 | J-leaded chip carrier |
| 3 | CQCC1-N28 | 28 | square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage to ground potential | -0.5 V dc to +7.0 V dc |
| DC voltage applied to outputs in High Z state | -0.5 V dc to +7.0 V dc |
| DC input voltage | -3.0 V dc to +7.0 V dc |
| Maximum power dissipation 2/ | 1.2 W |
| Lead temperature (soldering, 10 seconds) | +260ºC |
| Thermal resistance, junction-to-case ($\theta_{JC}$): | |
| Case outlines Y and 3 | See MIL-STD-1835 |
| Case outline X | 26ºC/W 3/ |
| Case outline Z | 20ºC/W 3/ |
| Junction temperature ($T_J$) | +175ºC |
| Storage temperature range | -65ºC to +150ºC |
| Temperature under bias | -55ºC to +125ºC |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Ground voltage (GND) | 0 V dc |
| Input high voltage ($V_{IH}$) | 2.2 V dc minimum |
| Input low voltage ($V_{IL}$) | 0.8 V dc maximum |
| Case operating temperature range ($T_C$) | -55ºC to +125ºC |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added $P_D$ due to short circuit test (e.g., $I_{OS}$).
3/ When the thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and verification provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -2.0 mA, $V_{IN} = V_{IH}, V_{IL}$ | 1, 2, 3 | All | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 8.0 mA, $V_{IN} = V_{IH}, V_{IL}$ | 1, 2, 3 | All | | 0.5 | |
| Input high voltage 1/ | $V_{IH}$ | | 1, 2, 3 | All | 2.2 | | |
| Input low voltage 1/ | $V_{IL}$ | | 1, 2, 3 | All | | 0.8 | |
| Input leakage current | $I_{IX}$ | $V_{IN}$ = 5.5 V to GND | 1, 2, 3 | All | -10 | 10 | µA |
| Output leakage current | $I_{OZ}$ | $V_{CC}$ = 5.5 V, $V_{OUT}$ = 5.5 V and GND | 1, 2, 3 | All | -40 | 40 | |
| Output short circuit current 2/ 3/ | los | $V_{CC}$ = 5.5 V, $V_{OUT}$ = 0.5 V | 1, 2, 3 | All | -30 | -90 | mA |
| Power supply current at frequency 3/ | $I_{CC1}$ | $V_{CC}$ = 5.5 V, $I_{OUT}$ = 0 mA, $V_{IN}$ = GND, f = $f_{MAX5}$ | 1, 2, 3 | All | | 200 | |
| Standby power supply current | $I_{CC2}$ | $V_{CC}$ = 5.5 V, $I_{OUT}$ = 0 mA, $V_{IN}$ = GND | 1, 2, 3 | All | | 150 | |
| Input capacitance 3/ | $C_{IN}$ | $V_{CC}$ = 5.0 V, $T_A$ = 25ºC, f = 1 MHz, (see 4.4.1c) | 4 | All | | 7 | pF |
| Output capacitance 3/ | $C_{OUT}$ | $V_{CC}$ = 5.0 V, $T_A$ = 25ºC, f = 1 MHz (see 4.4.1c) | 4 | All | | 8 | |
| Functional tests | | See 4.4.1d | 7, 8 | All | | | |
| Input to output propagation delay 5/ | $t_{PD}$ | 4/ | 9, 10, 11 | 01 | 3 | 40 | ns |
| | | | | 02 | 3 | 30 | |
| | | | | 03 | 4.6 | 25 | |
| Input register clock to output delay 6/ | $t_{ICO}$ | 4/ | 9, 10, 11 | 01 | | 65 | |
| | | | | 02 | | 50 | |
| | | | | 03 | | 45 | |
| Output data stable time from input clock 6/ | $t_{IOH}$ | 4/ | 9, 10, 11 | All | 5 | | |
| Input or feedback setup time to input register clock 6/ | $t_{IS}$ | 4/ | 9, 10, 11 | All | 5 | | |
| Input register hold time from input clock 6/ | $t_{IH}$ | 4/ | 9, 10, 11 | 01 | 20 | | |
| | | | | 02 | 15 | | |
| | | | | 03 | 13 | | |
| Input to input register asynchronous reset delay 6/ | $t_{IAR}$ | 4/ | 9, 10, 11 | 01 | | 65 | |
| | | | | 02 | | 50 | |
| | | | | 03 | | 45 | |
| Input register reset width 3/ 6/ | $t_{IRW}$ | 4/ | 9, 10, 11 | 01 | 65 | | |
| | | | | 02 | 50 | | |
| | | | | 03 | 45 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 4/<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input register reset recovery time 3/ 6/ | $t_{IRR}$ | | 9, 10, 11 | 01 | 65 | | ns |
| | | | | 02 | 50 | | |
| | | | | 03 | 45 | | |
| Input to input register asynchronous set delay 3/ 6/ | $t_{IAS}$ | | 9, 10, 11 | 01 | | 65 | |
| | | | | 02 | | 50 | |
| | | | | 03 | | 45 | |
| Input register set width 3/ 6/ | $t_{ISW}$ | | 9, 10, 11 | 01 | 65 | | |
| | | | | 02 | 50 | | |
| | | | | 03 | 45 | | |
| Input register set recovery time 3/ 6/ | $t_{ISR}$ | | 9, 10, 11 | 01 | 65 | | |
| | | | | 02 | 50 | | |
| | | | | 03 | 45 | | |
| Input and output clock width high 3/ 6/ 7/ 8/ | $t_{WH}$ | | 9, 10, 11 | 01 | 25 | | |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |
| Input and output clock width low 3/ 6/ 7/ 8/ | $t_{WL}$ | | 9, 10, 11 | 01 | 25 | | |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |
| Maximum frequency with feedback in input registered mode ($1/(t_{CO} + t_S)$) 3/ 9/ | $f_{MAX1}$ | | 9, 10, 11 | 01 | 14.2 | | MHz |
| | | | | 02 | 18.1 | | |
| | | | | 03 | 20.0 | | |
| Maximum frequency data path in input registered mode (Lower of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$ or $1/(t_{IS} + t_{IH})$) 3/ 6/ | $f_{MAX2}$ | | 9, 10, 11 | 01 | 15.3 | | |
| | | | | 02 | 20.0 | | |
| | | | | 03 | 22.2 | | |
| Output register clock to output delay 7/ | $t_{CO}$ | | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02 | | 30 | |
| | | | | 03 | | 25 | |
| Output data stable time from output clock 3/ 7/ | $t_{OH}$ | | 9, 10, 11 | 01-02 | 3 | | |
| | | | | 03 | 4.6 | | |
| Output register input set up time to output clock 7/ | $t_S$ | | 9, 10, 11 | 01 | 20 | | |
| | | | | 02, 03 | 15 | | |
| Output register input hold time from output clock 7/ | $t_H$ | | 9, 10, 11 | 01 | 12 | | |
| | | | | 02, 03 | 10 | | |
| Input to output register asynchronous reset delay 7/ | $t_{OAR}$ | | 9, 10, 11 | 01 | | 40 | |
| | | | | 02 | | 30 | |
| | | | | 03 | | 25 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

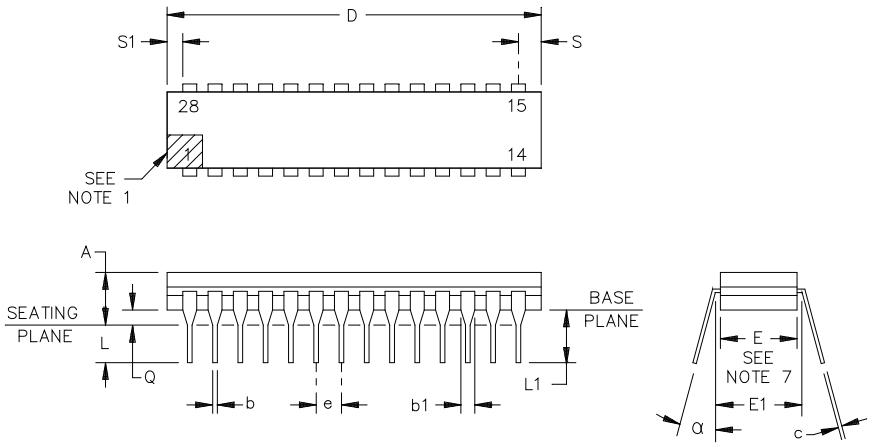
| Test | Symbol | Conditions 4/<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output register reset width 3/ 7/ | $t_{ORW}$ | | 9, 10, 11 | 01 | 40 | | ns |
| | | | | 02 | 30 | | |
| | | | | 03 | 25 | | |
| Output register reset recovery time 3/ 7/ | $t_{ORR}$ | | 9, 10, 11 | 01 | 40 | | |
| | | | | 02 | 30 | | |
| | | | | 03 | 25 | | |
| Input to output register asynchronous set delay 7/ | $t_{OAS}$ | | 9, 10, 11 | 01 | | 40 | |
| | | | | 02 | | 30 | |
| | | | | 03 | | 25 | |
| Output register set width 3/ 7/ | $t_{OSW}$ | | 9, 10, 11 | 01 | 40 | | |
| | | | | 02 | 30 | | |
| | | | | 03 | 25 | | |
| Output register set recovery time 3/ 7/ | $t_{OSR}$ | | 9, 10, 11 | 01 | 40 | | |
| | | | | 02 | 30 | | |
| | | | | 03 | 25 | | |
| Input to output enable delay 12/ 13/ | $t_{EA}$ | | 9, 10, 11 | 01 | | 40 | |
| | | | | 02 | | 30 | |
| | | | | 03 | | 25 | |
| Input to output disable delay 3/ 12/ 13/ | $t_{ER}$ | | 9, 10, 11 | 01 | | 40 | |
| | | | | 02 | | 30 | |
| | | | | 03 | | 25 | |
| Pin 14 to output enable delay 12/ 13/ | $t_{PZX}$ | | 9, 10, 11 | 01 | | 35 | |
| | | | | 02 | | 25 | |
| | | | | 03 | | 20 | |
| Pin 14 to output disable delay 3/ 12/ 13/ | $t_{PXZ}$ | | 9, 10, 11 | 01 | | 35 | |
| | | | | 02 | | 25 | |
| | | | | 03 | | 20 | |
| Maximum frequency with feedback in output registered mode 3/ 14/ 15/ | $f_{MAX3}$ | | 9, 10, 11 | 01 | 16.6 | | MHz |
| | | | | 02 | 22.2 | | |
| | | | | 03 | 25.0 | | |
| Maximum frequency data path in output registered mode (Lowest of $1/t_{CO}$, $1/t_{WH} + t_{WL}$) or $1/(t_S + t_H)$) 3/ 7/ | $f_{MAX4}$ | | 9, 10, 11 | 01 | 20.0 | | |
| | | | | 02 | 25.0 | | |
| | | | | 03 | 33.3 | | |
| Output data stable from output clock minus input register input hold time 3/ 16/ 11/ | $t_{OH} - t_{IH}$ | | 9, 10, 11 | All | 0 | | ns |
| Maximum frequency pipelined mode 3/ 8/ | $f_{MAX5}$ | | 9, 10, 11 | 01 | 18.5 | | MHz |
| | | | | 02 | 23.5 | | |
| | | | | 03 | 28.0 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second. $V_{OUT}$ = 0.5 V had been chosen to avoid test problems caused by tester ground degradation.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4, circuit A. See figure 6 for switching waveforms.
5/ Refer to figure 5, configuration 1.
6/ Refer to figure 5, configuration 2.
7/ Refer to figure 5, configuration 3.
8/ Refer to figure 5, configuration 6.
9/ Refer to figure 5, configuration 7.
10/ Refer to figure 5, configuration 9.
11/ This drawing is intended to guarantee interface compatibility of the other members of the device family; contact the manufacturer for compatibility information.
12/ Refer to figure 5, configuration 4.
13/ Measured at the point to which a previous high level has fallen to 0.5 V below $V_{OH}$ minimum or a previous low level has risen to 0.5 V above $V_{OL}$ maximum with the load in figure 4, circuit B. See figure 6 for enable and disable test waveforms.
14/ Refer to figure 5, configuration 8.
15/ This drawing is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source.
16/ Refer to figure 5, configuration 10.

Case X




CONFIGURATION 1

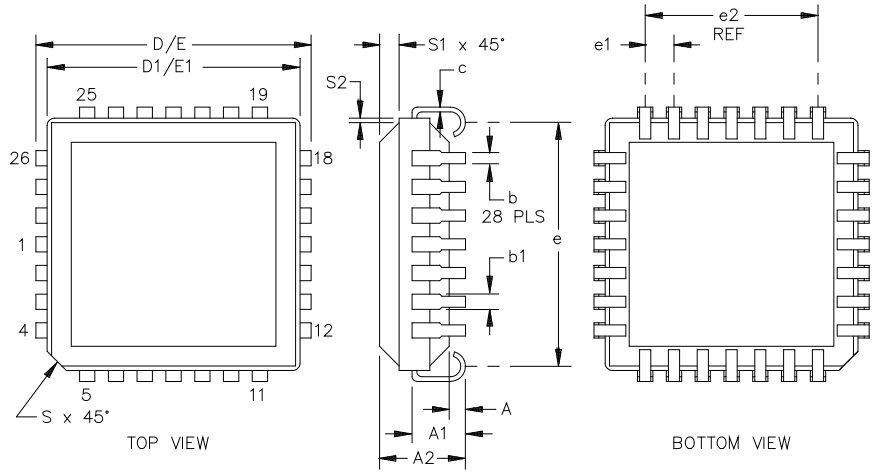
| | Inches | | Millimeters | | |
|---|---|---|---|---|---|
| Symbol | min | max | min | max | Notes |
| A | --- | .200 | --- | 5.08 | |
| b | .014 | .023 | 0.36 | 0.58 | 1 |
| b1 | .038 | .065 | 0.96 | 1.65 | 1, 2 |
| c | .008 | .015 | 0.20 | 0.38 | 1 |
| D | 1.430 | 1.485 | 36.33 | 37.72 | 3 |
| E | .220 | .310 | 5.59 | 7.87 | 3 |
| $E_1$ | .300 | .320 | 7.62 | 8.13 | 4 |

| | Inches | | Millimeters | | |
|---|---|---|---|---|---|
| Symbol | min | max | min | max | Notes |
| e | .100 BSC | | 2.54 BSC | | 5 |
| L | 1.25 | .200 | 3.19 | 5.08 | |
| $L_1$ | .150 | --- | 3.81 | --- | |
| Q | .015 | .060 | 0.38 | 1.52 | 6 |
| S | --- | .100 | --- | 2.54 | 7 |
| $S_1$ | .005 | --- | 0.13 | --- | 7 |
| α | 0º | 15º | 0º | 15º | |

NOTES:
1. All leads – Increase maximum limit by .003 (0.08 mm) measured at the center of the flat when lead finish A or B is applied.
2. The minimum limit for dimension $b_1$ may be 0.23 (0.58 mm) for leads numbers 1, 14, 15 and 28 only.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. Lead center when α is 0º. $E_1$ shall be measured at the centerline of the leads.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ± 0.10 (0.25 mm) of its exact longitudinal position relative to pins 1 and 28.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Applies to all four corners (leads number 1, 14, 15 and 28) shall apply.
8. Dimensions are in inches.
9. Metric equivalents are given for general information only.

FIGURE 1. Case Outlines.

Case Z




| | Inches | |
|---|---|---|
| Symbol | min | max |
| A | .035 | .045 |
| A1 | .090 | .120 |
| A2 | .155 | .180 |
| b | .017 | .021 |
| b1 | .026 | .032 |
| c | .035 | .045 |
| D / E | .485 | .495 |

| | Inches | |
|---|---|---|
| Symbol | min | max |
| D1 / E1 | .442 | .458 |
| e | .390 | .430 |
| e1 | .050 BSC | |
| e2 | .300 REF | |
| S | .040 BSC | |
| $S_1$ | .035 BSC | |
| S2 | .008 BSC | |

FIGURE 1. Case Outlines - Continued.

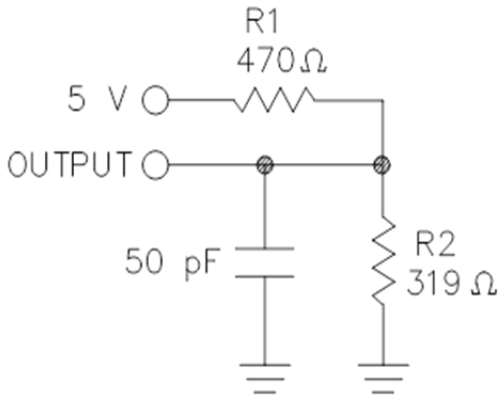
| Device Types | 01, 02 and 03 |
|---|---|
| Case Outlines | X, Y, Z and 3 |
| Terminal number | Terminal symbol |
| 1 | $I_0$ |
| 2 | $I_1$ |
| 3 | $I_2$ |
| 4 | $I_3$ |
| 5 | $I_4$ |
| 6 | $I_5$ |
| 7 | $I_6$ |
| 8 | GND |
| 9 | $I_7$ |
| 10 | $I_8$ |
| 11 | $I_9$ |
| 12 | $I_{10}$ |
| 13 | $I_{11}$ |
| 14 | $\overline{OE}$/ $I_{12}$ |
| 15 | $I/O_{11}$ |
| 16 | $I/O_{10}$ |
| 17 | $I/O_9$ |
| 18 | $I/O_8$ |
| 19 | $I/O_7$ |
| 20 | $I/O_6$ |
| 21 | GND |
| 22 | $V_{CC}$ |
| 23 | $I/O_5$ |
| 24 | $I/O_4$ |
| 25 | $I/O_3$ |
| 26 | $I/O_2$ |
| 27 | $I/O_1$ |
| 28 | $I/O_0$ |

FIGURE 2. Terminal connections.

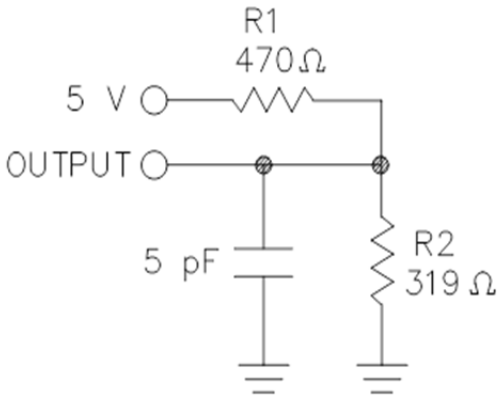
| Truth table | | | |
|---|---|---|---|
| Input pins | | Output pins | |
| $I_0$ | X | $I/O_{11}$ | Z |
| $I_1$ | X | $I/O_{10}$ | Z |
| $I_2$ | X | $I/O_9$ | Z |
| $I_3$ | X | $I/O_8$ | Z |
| $I_4$ | X | $I/O_7$ | Z |
| $I_5$ | X | $I/O_6$ | Z |
| $I_6$ | X | $V_{CC}$ | Z |
| $I_7$ | X | $I/O_5$ | Z |
| $I_8$ | X | $I/O_4$ | Z |
| $I_9$ | X | $I/O_3$ | Z |
| $I_{10}$ | X | $I/O_2$ | Z |
| $I_{11}$ | X | $I/O_1$ | Z |
| $\overline{OE}$/ I | X | $I/O_0$ | Z |

NOTES:
1. Z = High impedance
2. X = Don't care

FIGURE 3. Truth table (unprogrammed).




CIRCUIT A
OUTPUT LOAD
INCLUDING SCOPE AND JIG
(MINIMUM VALUES)




CIRCUIT B
OUTPUT LOAD FOR
($t_{EA}$, $t_{ER}$,
$t_{PZX}$ AND $t_{PXZ}$ ONLY)

AC test conditions

| | |
|---|---|
| Input pulse levels | GND to 3.0 V |
| Input rise and fall times | ≤ 5 ns |
| Input timing reference levels | 1.5 V |
| Output reference levels | 1.5 V |

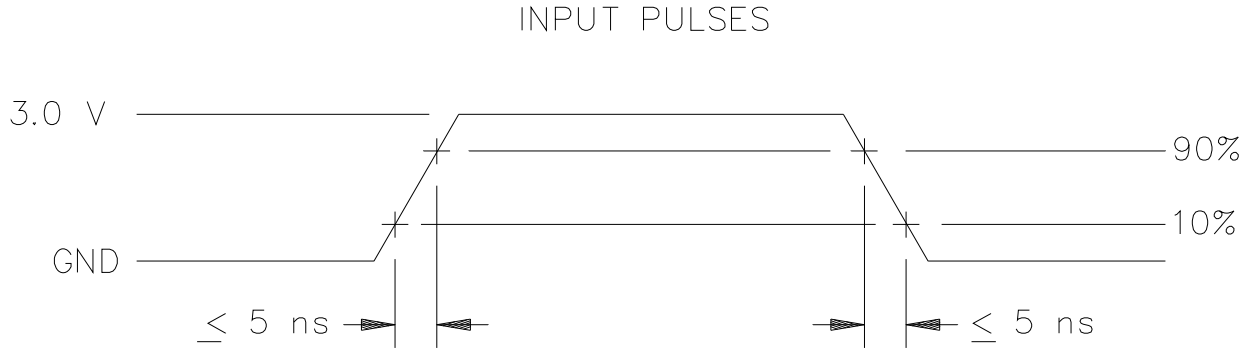



FIGURE 4. Output load circuit and test conditions.

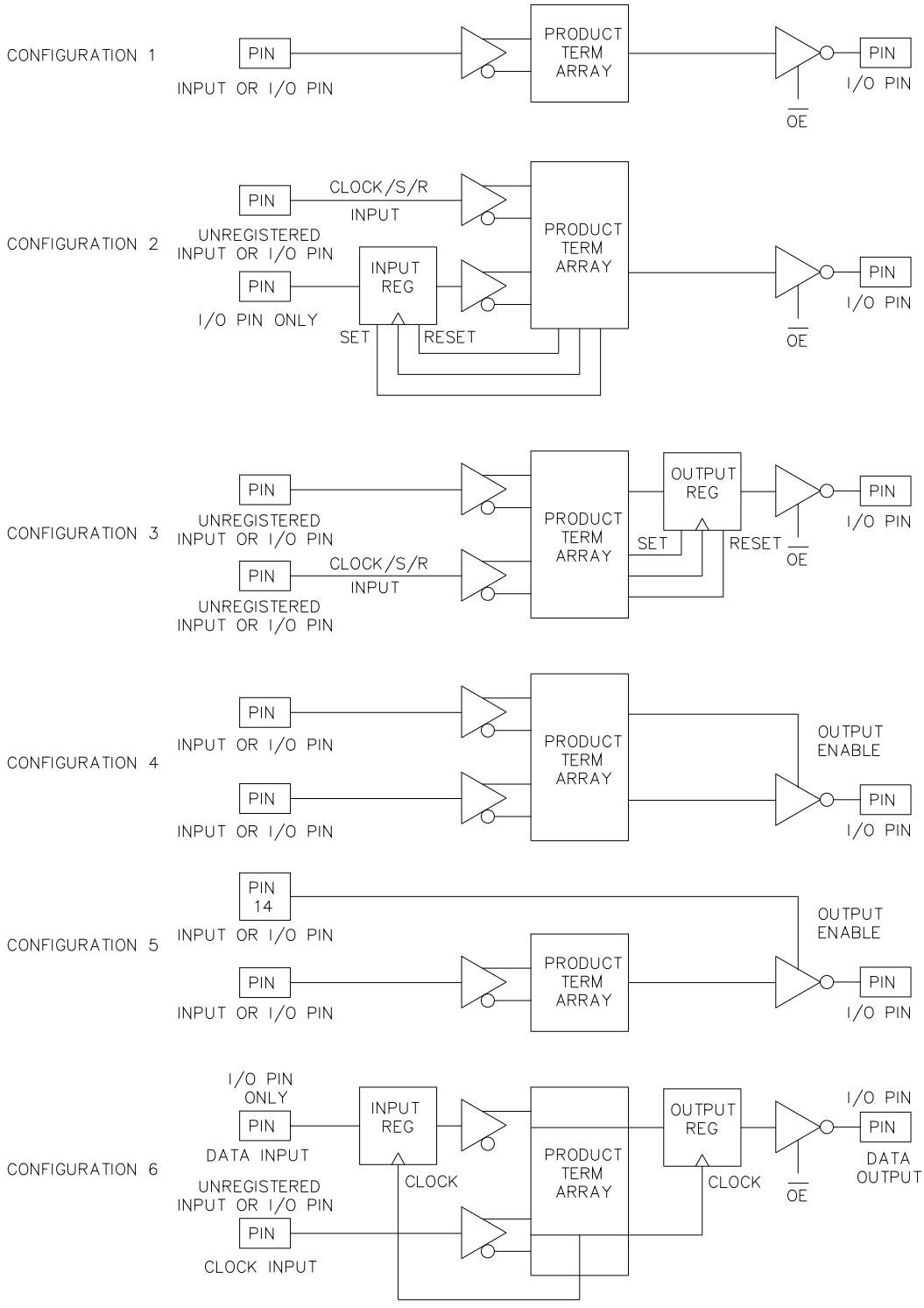



FIGURE 5. Timing configurations.

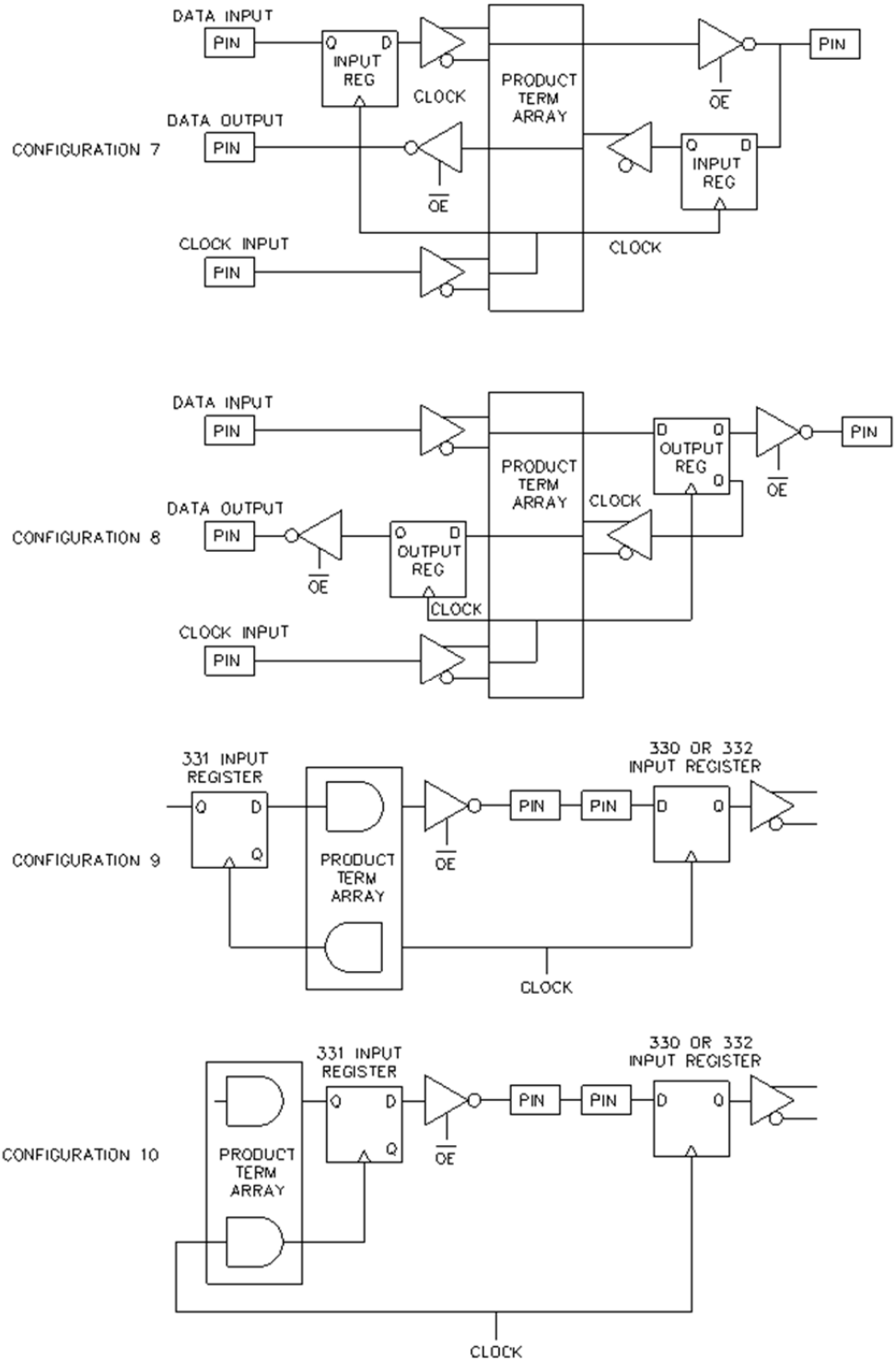
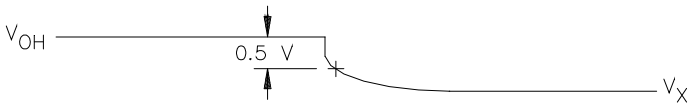
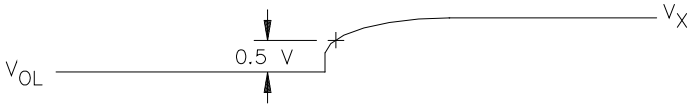
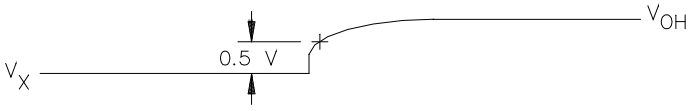
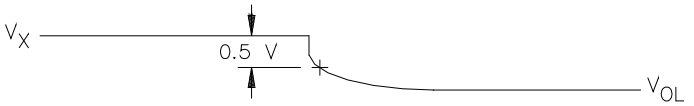



FIGURE 5. Timing configurations - Continued.

Output control switching waveform

| PARAMETER | $V_X$ | OUTPUT CONTROL SWITCHING WAVEFORM |
|---|---|---|
| $t_{PXZ}(-)$<br>$t_{ER}(-)$ | 1.5 V |  |
| $t_{PXZ}(+)$<br>$t_{ER}(+)$ | 2.6 V |  |
| $t_{PZX}(+)$<br>$t_{EA}(+)$ | 2.02 V |  |
| $t_{PZX}(-)$<br>$t_{EA}(-)$ | 2.02 V |  |

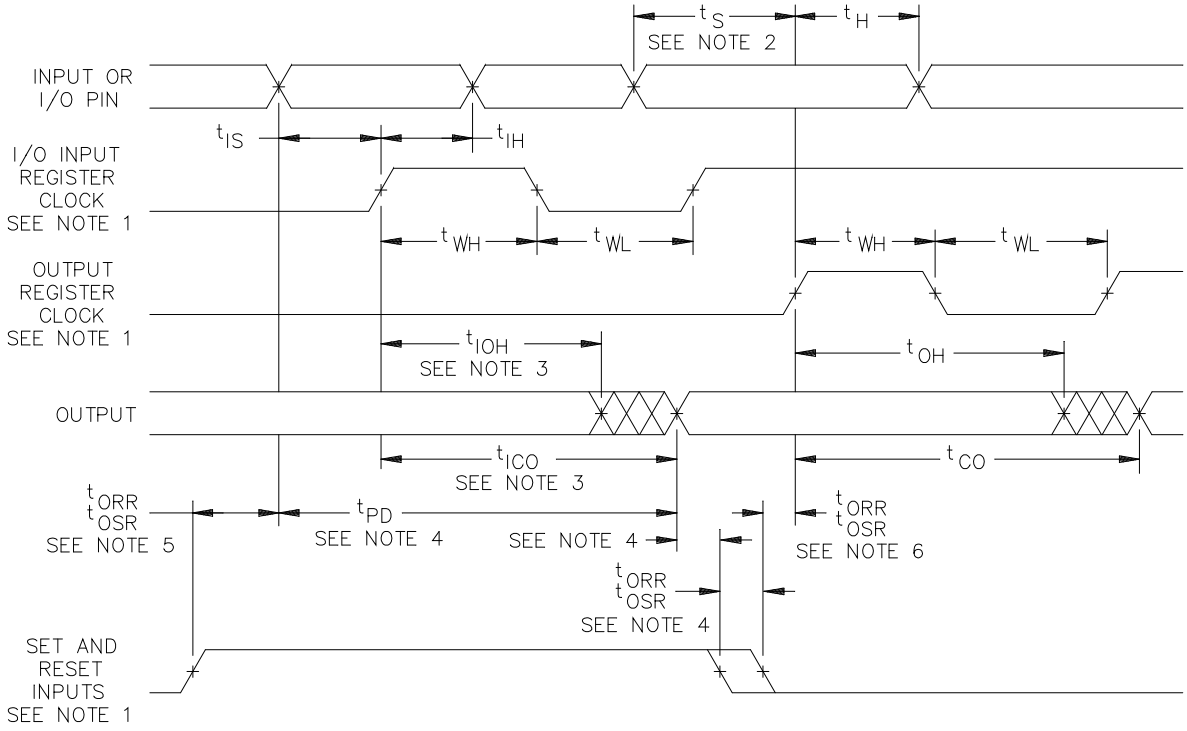
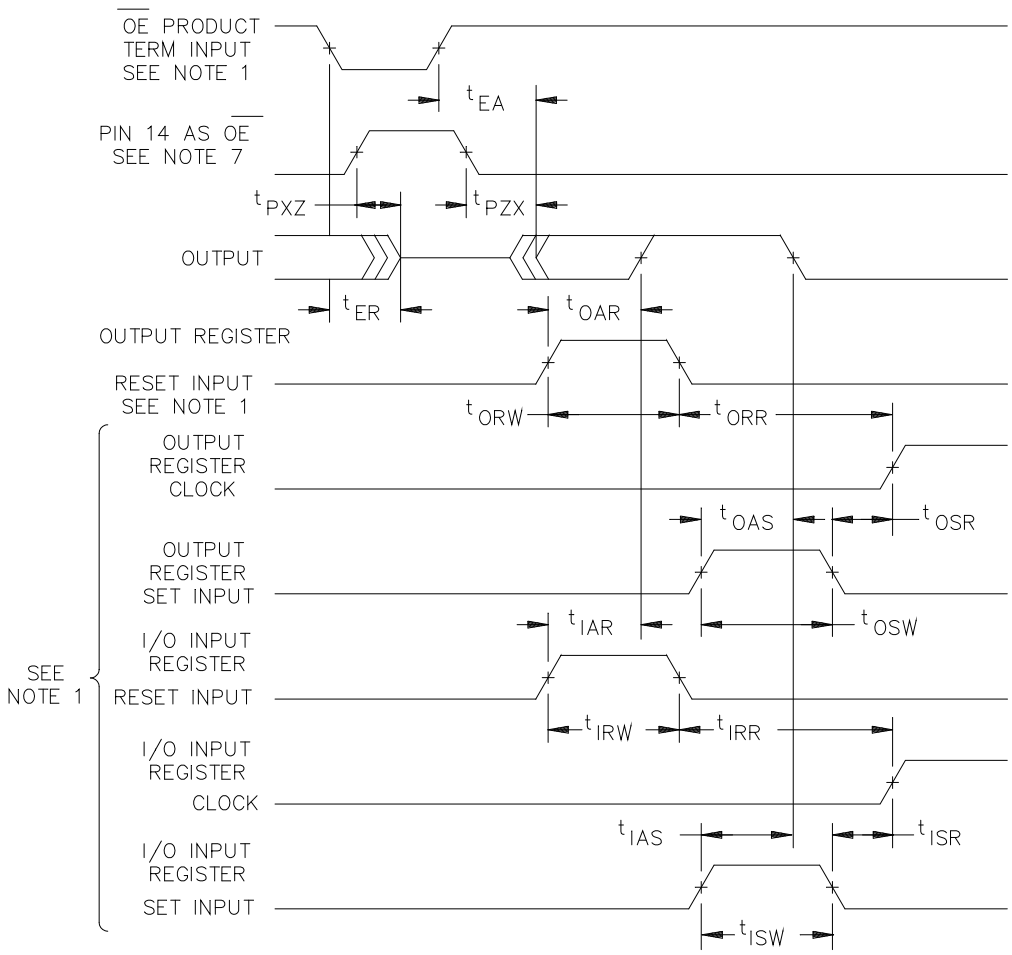



FIGURE 6. Switching waveforms.




NOTES:

1. As these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.
2. Dedicated input or input register set in transparent mode. Input register Set and Reset inputs are in a HIGH state.
3. Output register is set in transparent mode. Output register Set and Reset inputs are in a HIGH state.
4. Combinatorial Mode. Reset and Set inputs of the input and output registers should remain in a HIGH state at least until the output responds at $t_{PD}$. When returning Set and Reset inputs to a LOW state, one of these signals should go LOW a minimum of $t_{OSR}$ (Set input) or $t_{ORR}$ (Reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial Mode.
5. When entering the Combinatorial Mode, input and output register Set and Reset inputs must be stable in a HIGH state a minimum of $t_{ISR}$ or $t_{IRR}$ and $t_{OSR}$ or $t_{ORR}$ respectively prior to application of logic input signals.
6. When returning to the input and/or output Registered Mode, register Set and Reset inputs must be stable in a LOW state a minimum of $t_{ISR}$ or $t_{IRR}$ and $t_{OSR}$ or $t_{ORR}$ respectively prior to the application of the register clock input.
7. Refer to figure 6, configuration 5.

FIGURE 6. Switching waveforms - Continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

| Line no. | Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|---|
| | | Device class M | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | | |
| 2 | Static burn-in method 1015 | Not required | Not required | Not required |
| 3 | Same as line 1 | | | |
| 4 | Dynamic burn-in (method 1015) | Required | Required | Required |
| 5 | Same as line 1 | | | |
| 6 | Final electrical parameters (programmed devices) | 1*, 2, 3, 7*, 8A, 8B | 1*, 2, 3, 7*, 8A, 8B | 1*, 2, 3, 7*, 8A, 8B |
| 7 | Group A test requirements | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| 8 | Group C end-point electrical parameters | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B | |
| 9 | Group D end-point electrical parameters | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B |
| 10 | Group E end-point electrical parameters | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II).

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1c.

6/ The device manufacturer may at his option, either complete subgroup I electrical parameter measurements within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table II herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for the initial characterization and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

e. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10 and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10 and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9, 10 and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125ºC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-10-31

Approved sources of supply for SMD 5962-89855 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8985501MXA | 3/ | CY7C331-40DMB |
| 5962-8985501MYA | 3/ | CY7C331-40KMB |
| 5962-8985501MZA | 3/ | CY7C331-40YMB |
| 5962-8985501M3A | 3/ | CY7C331-40LMB |
| 5962-8985502MXA | 3/ | CY7C331-30DMB |
| 5962-8985502MYA | 3/ | CY7C331-30KMB |
| 5962-8985502MZA | 3/ | CY7C331-30YMB |
| 5962-8985502M3A | 3/ | CY7C331-30DLB |
| 5962-8985503MXA | 3/ | CY7C331-25DMB |
| 5962-8985503MYA | 3/ | CY7C331-25KMB |
| 5962-8985503MZA | 3/ | CY7C331-25YMB |
| 5962-8985503M3A | 3/ | CY7C331-25LMB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. Last known source is listed below.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 65786 | Cypress Semiconductor<br>198 Champion Court<br>San Jose, CA 95134-1709 |